MODEL 532
Intelligent Logic State Analyzer

Features:

- **Provides 32 channels, 250 words of storage and 21 triggering modes.**
- **Displays data in hexadecimal or binary.**
- **Computes and displays "signature" of data collected.**
- **Offers auxiliary memory for PROM and RAM storage of 8 internal tests for automatic operation.**
- **Permits remote operation through RS-232 or IEEE-488 interfaces.**
- **Provides active control of various microprocessors.**

PARATRONICS, INC.

MODEL 532

The Model 532 is a compact, 32-channel microprocessor-based logic state analyzer whose internal bus structure permits the addition of special features by inserting small applications boards.

Basic Features

The basic Model 532 captures up to 250 words. The 32 channels associated with each word can be operated together or functionally split into "A" and "B" groups, each 16 bits wide and each separately clocked. One application of this approach is the support of systems designed around the latest generation of microprocessor chips which use different clocks to multiplex address and data on the same pins.

In the stand-alone mode, keyboard commands allow the choice of the trigger word, or one line of data, or two "signatures" to be displayed in hexadecimal readouts at the left of the unit as shown in Figure 1. The location of the data word is always displayed in the readouts at the right. The signatures reflect a software-implemented comparison of the entire memory contents and "compress" these contents into two hexadecimal words for a quick summary of the data collected. Thus, if even a single bit changes between data collections, this change will be immediately apparent by the display of a different signature.

If a 16-line truth table or "page" presentation is preferred, the Model 532 can be used with an ordinary lab or field oscilloscope. The hexadecimal and binary displays available are shown in Figure 2. These presentations include the signatures and the location of the truth table relative to the trigger word. All 16 pages in the data memory can be examined sequentially using a control on the front panel.

Oscilloscope and pod connections are shown in Figure 3. There are three pod types available: fixed threshold (TTL), variable threshold (±12V), and the dedicated personality pods for microprocessor control and program development. Each dedicated pod permits SINGLE STEP, RUN, HALT, BREAKPOINT, and READ/WRITE functions. The basic Model 532 also incorporates a calculator-type keyboard for entering the desired triggering and delay modes. As an example of one of the 21 powerful modes available, the analyzer can be programmed to trigger on the occurrence of one event and the *nonoccurrence* of a second expected but intermittent event. This

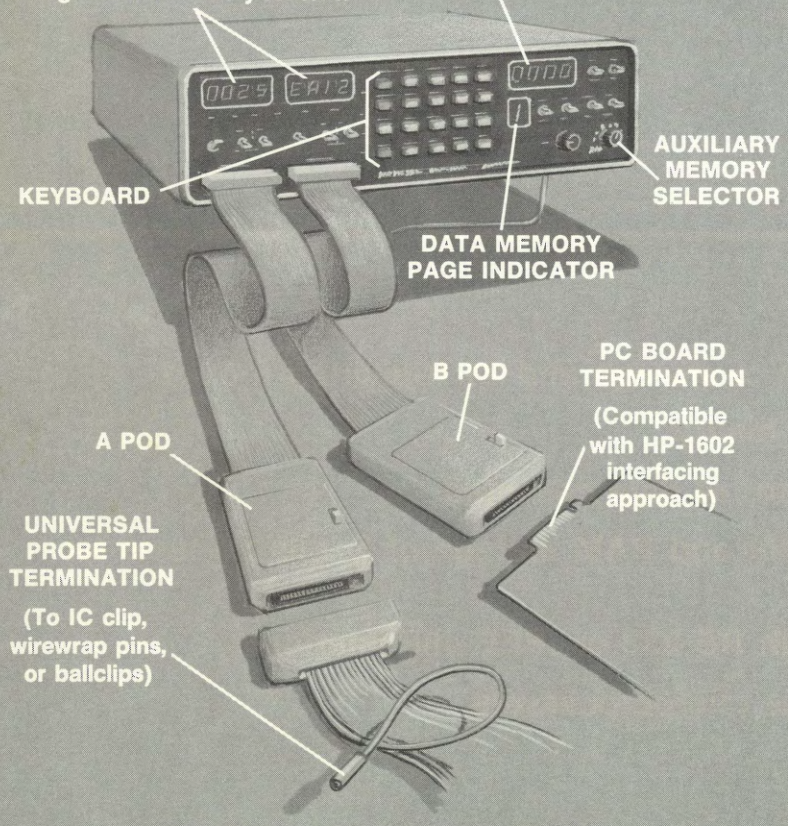

A and B GROUP READOUTS
Each readout represents 16 bits and displays choice of:
■ Trigger word
■ Data in memory
■ Signature of memory contents
DATA WORD LOCATOR
Readout displays choice of:
■ Location of data word in analyzers memory relative to trigger
■ Clock or trigger delay used
KEYBOARD
AUXILIARY MEMORY SELECTOR
DATA MEMORY PAGE INDICATOR
B POD
PC BOARD TERMINATION
(Compatible with HP-1602 interfacing approach)
A POD
UNIVERSAL PROBE TIP TERMINATION
(To IC clip, wirewrap pins, or ballclips)

FIGURE 1. Stand Alone Mode

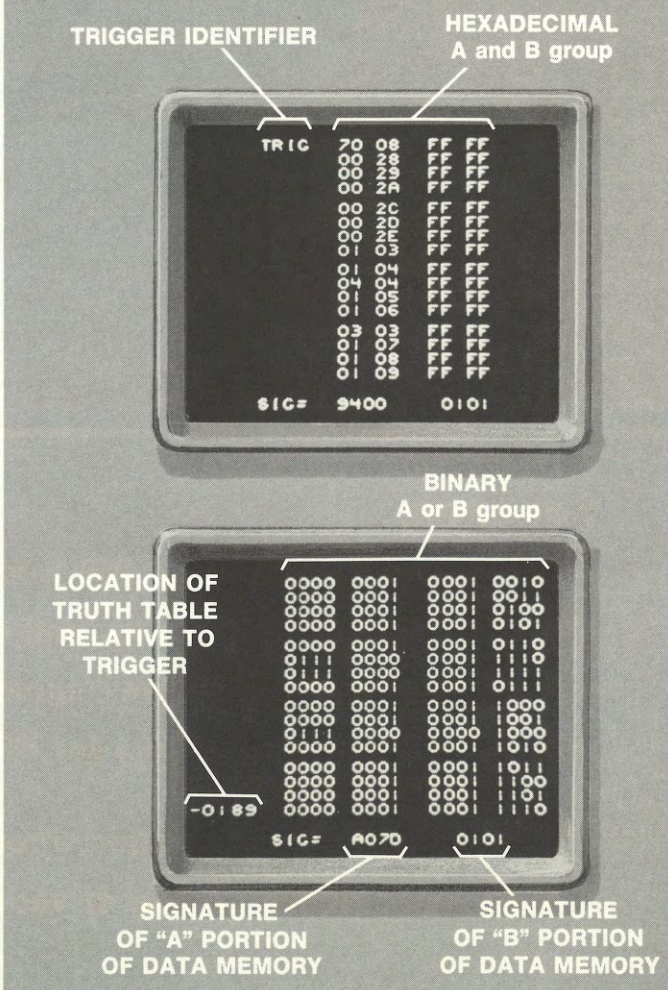

TRIGGER IDENTIFIER
HEXADECIMAL A and B group
TRIG
SIG= 9400 0101
BINARY A or B group
LOCATION OF TRUTH TABLE RELATIVE TO TRIGGER
-0189
SIG= A070 0101
SIGNATURE OF "A" PORTION OF DATA MEMORY
SIGNATURE OF "B" PORTION OF DATA MEMORY

FIGURE 2. Typical Scope Presentations

Intelligent Logic State Analyzer

type of triggering can pinpoint the intermittent problem even when the failure mode is unknown since the analyzer will collect and display only when the anomaly occurs.

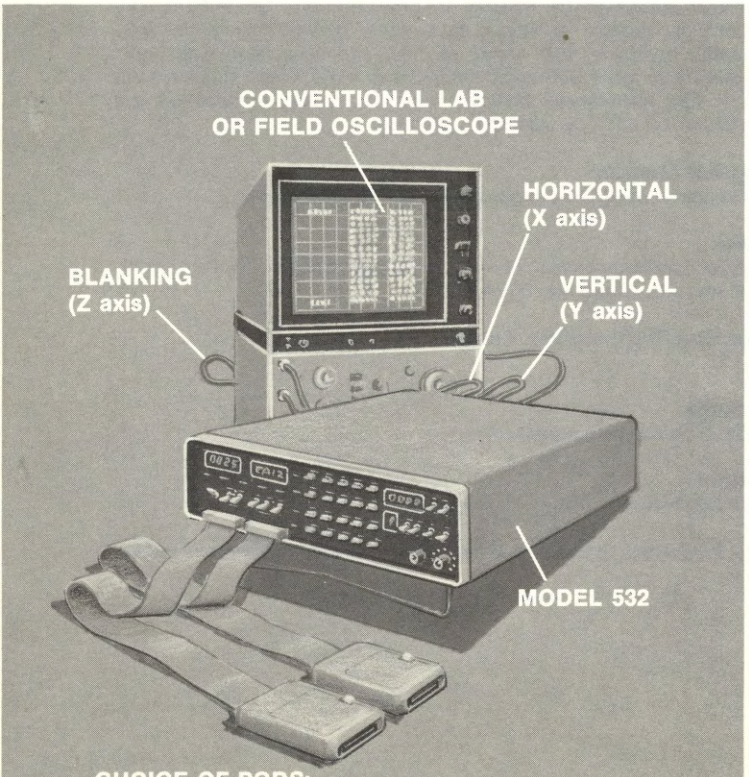
Additional features of the basic instrument include: a 5 MHz data memory, pre-trigger and post-trigger data collection, independent A and B trigger and clock qualifiers, up to 10,000 steps of digital delay for program paging and loop analysis, and an automatic self-test each time the Model 532 is turned on.

Add-On Features

In situations where additional capability is required, the following application boards can be plugged into the analyzer's internal bus:

- ☐ *12 MHz Data Memory Board* — Permits data collection as high as 12 million 32-bit words per second. (Factory installed.)
- ☐ *Auxiliary Memory Board* — Permits up to eight tests to be performed with minimum operator intervention. Information transferred from main to auxiliary memory includes 250 data words, the associated signatures, and the front panel settings used in the original data collection. Upon recall of a particular test, the analyzer takes over front panel control, automatically collects new data, and highlights any differences between the main and auxiliary memories. The Auxiliary Memory Board contains one RAM for temporary storage, seven UV PROMs for "semi-permanent" storage, and PROM programming circuitry. PROMs are programmed by the Model 532 only if they are blank and if the proper keystroke sequence is executed.
- ☐ *RS-232 Interface Board* — Permits hardcopy of test results; allows two-way communication over a modem from a remote computer for automated test control and analysis; and supports downloading of programs for microprocessor development applications when the dedicated pod is used.
- ☐ *IEEE-488 Interface Board* — Same functions as above when a IEEE-488 computer/controller is used.

Figure 4 illustrates the implementation of a fully-automated logic state analysis system.



CHOICE OF PODS:

- **Fixed Threshold at 1.6V with hysteresis; low-power Schottky load; accepts logic swings between −0.5V and +15V.**
- **Variable Threshold; input impedance: 50K Ω, 15pF; threshold variable between ±12.0V.**
- **Dedicated Pod; terminated in 40-pin dip clip; provides active control of microprocessor I.C.**

FIGURE 3. Analyzer Interconnections

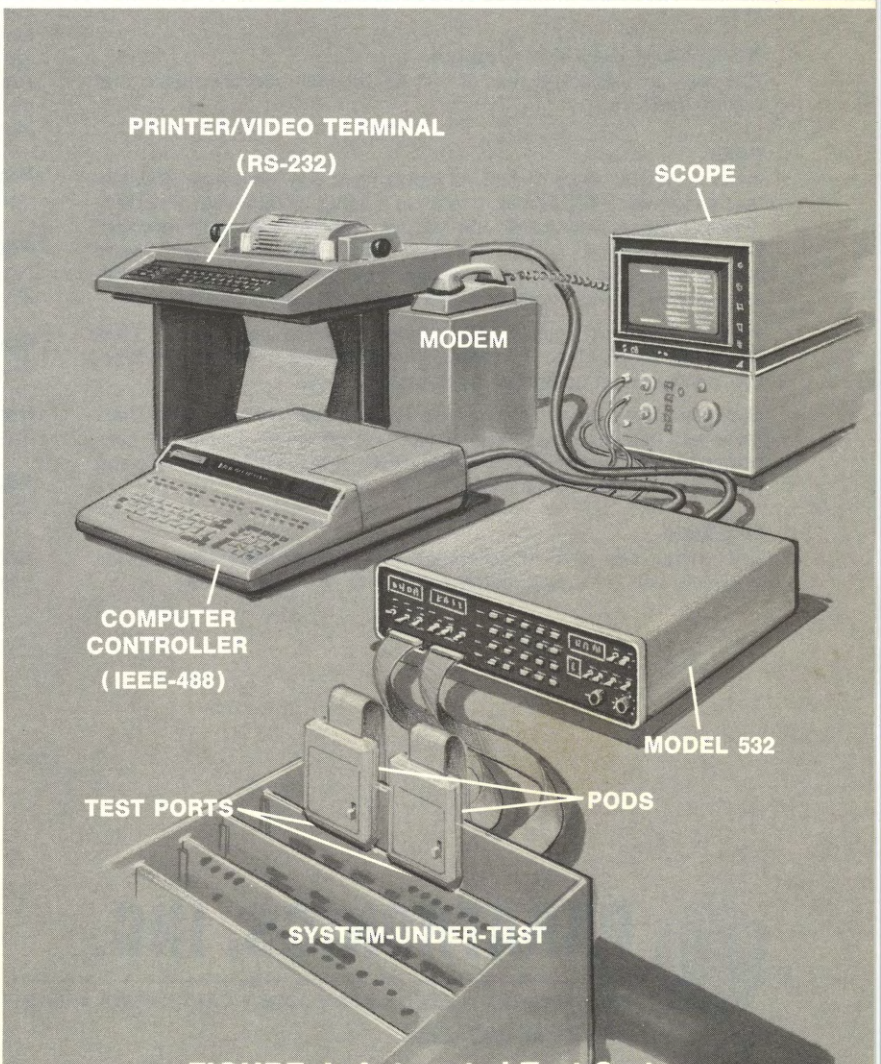


FIGURE 4. Automated Test System

Specifications

Physical
3.5" high x 12" wide x 13¾" deep; 8 pounds.

Display
Trigger word, data, signatures, page indicator and digital delay relative to trigger on self-contained LED readouts; or oscilloscope display provides same information along with data in sixteen selectable 16-line hexadecimal or binary truth table "pages."

Real-Time Data Collection
250 words, each 32 bits wide. Data memory organized as two 16-bit data groups (A and B). Each data group has independent input clocks and trigger and clock qualifiers.

Input Clocks
Maximum clock rate is 5 MHz with standard memory or 12 MHz with optional high-speed memory. Rising or falling clock edge can be selected independently for A or B group; or both groups can be clocked together from A clock. Minimum clock pulse width is 20 ns at threshold.

Oscilloscope Requirements
Input sensitivity (X and Y): 1V/division min.; bandwidth: 500 KHz min.; X, Y phase shift: $\leq 10°$ at 300 KHz; blanking (Z axis): fully blanked by positive or negative pulse, 30V or less. Analyzer provides required X, Y, Z outputs using BNC connectors at rear of unit.

External Sync Output
BNC connector at rear of unit provides TTL pulse when all triggering requirements are met.

Trigger Bus
Connector at rear of unit expands analyzer triggering beyond 32 bits.

RS-232 and IEEE-488 Outputs
Standard connectors at rear of unit for two-way communication and control functions.

Pods
Fixed Threshold Type (1.6V): All inputs have one low-power Schottky load as follows: −400ua max. (−0.5V to +0.9V); +100ua max (+2.0V to +15.0V). Inputs incorporate 400 MV min. hysteresis for noise rejection. Input capacitance < 20pF at pod head. Switch on pod inverts (compliments) all data and qualifiers. Pod accepts probe head with color-coded "flying" leads or plugs directly into system at test port.

Variable Threshold Type (±12.0V range): All inputs have 50K Ω, 15pF input impedance. Fixed TTL threshold (1.6V) is also provided. Pod interfaces with system-under-test as described above.

Dedicated Pod: Input load same as Fixed Threshold Type. Pod interfaces with microprocessor-under-test using dedicated 40-pin DIP connector and provides SINGLE STEP, RUN, HALT, BREAKPOINT, and memory READ/WRITE functions.

Qualifiers
Both trigger and clock qualifiers are provided for each 16-bit group. Qualifiers can be independently set to 1, 0, or X (don't care).

Set-Up and Hold Times
Set-up time for data and qualifiers prior to selected clock edge is 30 ns. Hold time for data and qualifiers after selected clock edge is 0 ns.

Delay
Up to 10,000 clock or trigger events.

Triggering Modes
General: Analyzer triggering is specified by the A and B data groups. Each group is defined by keyboard entry of 0 to 4 hexadecimal characters. Provides pre-trigger and post-trigger data capture. Delay, if any, can be on n trigger or clock events, where $0 \leq n \leq 9999$.

Parallel Modes: (A,B) refers to a full 32-bit wide trigger word. (A,$\overline{B}$)DLY: Trigger when (A,B) occurs and delay condition is satisfied. (A,$\overline{B}$)DLY: Trigger when A and any word other than B occurs and delay condition is satisfied.

Sequential Modes: (A=B) refers to two trigger words in the A data group. A is the trigger word that must occur first; B is the trigger word that must occur second. In this mode, the B data inputs have no effect on triggering. Full 32-bit data collection and display still occurs.

(A,DLY=B): Trigger when B occurs exactly n clock or trigger delay events from A.

(A,DLY=$\overline{B}$): Trigger when any event other than B occurs exactly n clock or trigger delay events from B.

(A,DLY ≥ B): Trigger when B occurs n or more delay events from A.

Start A/Stop B: Start data collection when A occurs; stop collection when B occurs. If more than 250 data words are collected, the most recent set of 250 words are stored.

Auxiliary Memory
One RAM and seven UV PROMs are provided. Each of the 8 memory elements is capable of storing front panel control settings for later automatic operation, 250 words of data, and associated signatures. PROMs are programmed by Model 532 only if blank and can be erased by UV light. Differences between main and auxiliary memories are highlighted on CRT by alternating displays.

Program Memory
Can be user-defined and expanded for special applications.

Power
Analyzer uses wide-range, high-efficiency power supply: 90-135V/180-270V rms AC; 50/60 Hz; 60VA max.

Operating Temperature Range
0-50°C.

Humidity
0-95% R.H. with no condensation.

Altitude
To 10,000 feet.

Note: Paratronics, Inc. reserves the right to change specifications without notice.

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